# Lecture 5 Learning outcomes

Upon successful completion of this module, you will be able to:

# Define and describe functionalities of logical units for integer operations add, sub, and, or.

# Design and trace multiplication unit.

# Represent FP numbers in IEEE 754 representations.

# Describe the algorithm and hardware diagram of FP addition

# Design an FP multiplication unit.

# Lecture 5 Activities

Lecture 5 study is split into 3-day work with the 4th day of the week designated for Test 2.

**Day 1:**

Session I:

     View Lecture 5a: ALU

     Study zyBook 3.1 & 3.2

Session II:

View Lecture 5b: Integer Multiplication

Study zyBook 3.3  
Session III:

Recap and practice (selected H3 problems)  
**Day 2:**

Session I:

View Lecture 5c: IEEE 754 FP representations  
 Study zyBook 3.5 (FP representation part, i.e. read up to but not include FP addition)  
Session II:

View Lecture 5d: FP addition  
 Study zyBook 3.5 (Floating-Point addition).  
Session III:

Recap and practice

Work on Homework H3  
**Day 3**

Session I:

View Lecture 5e: FP multiplication.

Study zyBook 3.5 (complete the whole section 3.5).  
Session II:   
 Read zyBook 3.9 (exercise not required.)

Session III: (50 minutes)  
 Review and Catchup

Complete Homework H3

Day 4

Review, study and take Test 2.

**Assignment Checklist:** -- due Th 6/17

Z5: zyBook 3.1-3.3

Z6: zyBook 3.5

H3: Homework #3

Take Test 1 between 6/17 – 6/20